REMARKS/ARGUMENTS

Favorable reconsideration of this application in light of the following discussion is respectfully requested.

Claims 1-12, and 15-21 are pending. Claim 19 is amended. No new matter is added.

The outstanding Office Action objected to Claim 19 for informalities. In addition, Claims 1-3, 5, 7, 8, 11, and 15-19 were rejected under 35 U.S.C. § 103(a) as unpatentable over Byers (U.S. Patent No. 6,906,407) in view of Nagesh (U.S. Patent No. 5,585,671). Claims 4, 6, 9, 10, and 12 were objected to as dependent upon a rejected base claim, but indicated as allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims, and Claims 20 and 21 were indicated as allowed.

The indication of allowed and allowable subject matter is gratefully acknowledged. For the reasons discussed below, all of the claims are believed to be in condition for allowance.

The outstanding Office Action objected to Claim 19 because the recitation of "the thermal coupling" lacks antecedent basis. In response to the objection, Claim 19 is amended to recite "a thermal coupling." In view of its formal nature, this amendment does not raise a question of new matter. The amendment to Claim 19 is believed to overcome the outstanding objection, and it is respectfully requested that the objection to Claim 19 be withdrawn.

The rejection of Claims 1-3, 5, 7, 8, 11, and 15-19 under 35 U.S.C. § 103(a) as unpatentable over Byers in view of Nagesh is respectfully traversed.

Independent Claim 1 relates to an LSI package arranged on a mounting board and configured to be provided with a heat dissipation member. Claim 1 recites:

> ...the LSI having signal input and output terminals and a surface to be coupled to the heat dissipation member...
> ...a package structure configured to hold the signal transmission lines and the second coupling parts... the package structure being mounted on the interposer and having a space for receiving the LSI to allow the heat dissipation member to be located above the surface of the LSI. [Emphasis Added]

Independent Claim 3 relates to an LSI package arranged on a mounting board and having a configuration for mounting a heat dissipation member. Claim 3 recites:

> ... the LSI having signal input and output terminals and a surface to be coupled to the heat dissipation member...
> ...a package structure configured to hold the signal transmission lines and the second coupling parts, the package structure being mounted on the interposer and having a space for receiving the LSI to allow the heat dissipation member to be located on the surface of the LSI... [Emphasis Added]

The combination of Byers and Nagesh fails to disclose or suggest the claimed package having a space for receiving an LSI to allow a heat dissipation member to be located on the surface of the LSI.

Figure 2 of Byers illustrates a gate array assembly (100). The gate array assembly (100) includes a bottom integrated circuit (102) and a top integrated circuit (104).[1] The bottom integrated circuit (102) and top integrated circuit (104) are electrically and mechanically coupled together.[2] Bottom integrated circuit (102) includes a cavity-up ball grid array package (107) that is electromechanically coupled to printed circuit board (106).[3] An integrated circuit (IC) die (10) is coupled to package (107) in a flip chip style via solder balls (112).[4]

[1] See Byers, at col. 3, lines 5-7.
[2] See Byers, at col. 3, lines 7-10.
[3] See Byers, at col. 3, lines 43-49.
[4] See Byers, at col. 4, lines 1-2.

The outstanding Office Action appears to acknowledge the absence of a package having a space for receiving an LSI to allow a heat dissipation member to be located on the surface of the LSI in the gate array assembly of Byers, stating "Byers does not specific [sic] disclose a package structure (a heat sink) configured to hold the signal lines and the second coupling parts, the structure being mounted on the interposer and having space."[5] The outstanding Office Action asserts that Nagesh cures the deficiency in Byers, stating:

> Nagesh shows a package figure 1 comprising a package structure or a heat sink configured to hold a signal line of signal lines and mounted on an interposer (14) having space.
>
> It would have been obvious to one having ordinary skill in the art at the time the invention was made to have a heat sink structure as taught by Nagesh employed in the LSI package of Byers in order to provide a cooling system and heat dissipation for the package.[6]

Applicants respectfully disagree. M.P.E.P. § 2143.01(V) states that "[I]f proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification."[7] In this case combining the heat sink structure of Nagesh with the IC die (10) of Byers would render the gate array assembly of Byers unsatisfactory for its intended purpose. Specifically, including the heat sink structure of Nagesh in the gate array assembly of Byers would prevent the bottom integrated circuit (102) of Byers from electrically and mechanically coupling to the top integrated circuit (104) of Byers.

Figure 1 of Nagesh illustrates a thermal resistance package for a high power flip chip ICS. A flip chip IC package (10) includes an integrated circuit chip or die (12) mounted on a substrate (14).[8] Solder bumps form interconnects between circuitry formed on an inverted interconnect side of the chip (12) and the upper side of the substrate (14).[9] The substrate (14)

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[5] See the outstanding Office Action at page 2.
[6] See the outstanding Office Action at page 3, lines 1-7.
[7] See also *In re Gordon*, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984)
[8] See Nagesh,, at col. 4, lines 14-17.
[9] See Nagesh,, at col. 4, lines 17-20.

includes electrical connections (26) that coupling the package to a printed circuit board (28).[10] A heat sink frame (30) is mounted on the printed circuit board (28) to receive a heat sink (32).[11] A heat sink-lid interface layer (34) and heat sink support structure (36) provide a thermal connection between the lid (20) and the heat sink (32).[12]

Thus, combining the heat sink structure of Nagesh with the gate array assembly of Byers would include placing the heat sink frame (30) Nagesh on the printed circuit board (106) of Byers. The heat sink (32) would then be placed on the heat sink frame (30). However, such an arrangement would not allow the IC (10) of Byers to be coupled to the heat sink (32) because the top integrated circuit (102) would get in the way. Stated another way, including the heat sink frame (30) and the heat sink (32) of Nagesh so that they were coupled to the IC (10) of Byers would interfere with the assembly of the bottom integrated circuit (102) to the top integrated circuit (104) of Byers. However, Byers identifies a problem with conventional devices and states that:

> The need is met and an advance in the art is accomplished by a new class of integrated circuit assemblies in accordance with the present invention. In particular a programmable integrated circuit (IC) is combined with an integrated circuit or other device to offer the flexibility of programmability with functionality and/or electrical performance characteristics typically unavailable in a programmable IC.[13]

Preventing the combination of the bottom integrated circuit (102) with the top integrated circuit (104) by including the heat sink assembly of Nagesh would render the gate array assembly of Byers unsatisfactory for the stated intended purpose. Therefore there is no motivation to combine the heat sink structure of Nagesh with the gate array assembly of Byers.

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[10] See Nagesh, at col. 4, lines 34-37.
[11] See Nagesh, at col. 4, lines 37-39.
[12] See Nagesh, at col. 4, lines 39-42.
[13] See Nagesh, at col. 1, lines 50-56 (emphasis added).

Accordingly, even the combined teachings of Byers and Nagesh fail to disclose or suggest the features of independent Claims 1 or 3. It is submitted that independent Claims 1 and 3 and the claims depending therefrom are in condition for allowance.

For the foregoing reasons, it is respectfully submitted that this application is now in condition for allowance. A Notice of Allowance for Claims 1-12, and 15-21 is earnestly solicited.

Should the Examiner deem that any further action is necessary to place this application in even better form for allowance, he or she is encouraged to contact Applicant's undersigned representative by the below listed telephone number.

Respectfully submitted,

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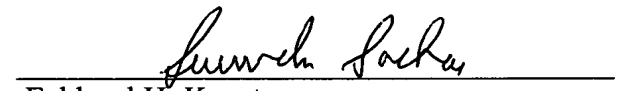
MAIER & NEUSTADT, P.C.



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